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EXAMINER	
MERED, HABTE	

ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,968	STEVEN G SCHMIDT	
	Examiner	Art Unit	
	Habte Mered	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 12/19/2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 03/12/2002.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claim 18** is rejected under 35 U.S.C. 102(b) as being anticipated by Yamada (US 5, 455, 820).

Yamada teaches an ATM switch that is both input and output buffered. Yamada's system provides spare buffer to store data intended for an output that is temporarily unable to accept data addressed to it. In Yamada's system Head Of Line Blocking is addressed by using spare buffers.

Yamada discloses a method for temporarily deferring transmission of packets/frames to a destination port in a buffered switch, comprising the steps of: receiving a request for transmission of at least one packet/frame to the destination port **(Column 3, Lines 30-34 and also see Figure 1 item 30)**; determining whether the destination port is available to receive the at least one packet/frame **(Column 3, Lines 40-45 and item 50N in Figure 1. The destination port sends a signal indicating buffer occupancy level)**; deferring transmission of the at least one packet/frame when the destination port is not available to receive the at least one packet/frame **(Column 4, Lines 50-55 and S16 in Figure 4A)**; and repeating the above steps for a next packet/frame to be transmitted **(See Figures 4A and 4B)**.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1 and 2** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US 5, 455, 820) in view of Yamanaka et al (US 5, 619, 495), hereinafter referred to as Yamanaka.

5. Regarding **claim 1**, Yamada teaches a buffer control apparatus **(See Figure 3, element 120)** in a buffered switch for controlling transmission of packets/frames of data with a deferred queue device to temporarily defer transmission of the packets/frames to a destination port which is unavailable to receive the packets/frames. **(Yamada in Figure 3 shows the deferred queue as cell buffers 140_2 and 140_3. See also Column 4, Lines 50-67.)**

Yamada fails to disclose that the buffers used are a dual port buffer memory for storing the packets/frames of data; a buffer write module for writing packets/frames into the dual port buffer memory; a buffer read module for reading packets/frames of data from the dual port buffer memory.

Yamanaka discloses a cell switching system having buffer memories in which accesses of a plurality of cells can be implemented in one cell time.

Yamanaka teaches a system with a control buffer **(Figure 1, element 15)** and the buffers used are a dual port buffer memory for storing the packets/frames of data; a

buffer write module **(Figure 1, element 16)** for writing packets/frames into the dual port buffer memory; a buffer read module **(Figure 1, element 19)** for reading packets/frames of data from the dual port buffer memory. **(Yamanaka further shows that in Figure 13 the buffer can be a dual port buffer memory. See also Column 16, Lines 20-30)**

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify Yamada's system by incorporating dual port buffer memory with read and write module so that the read out and writing can be performed simultaneously to increase ports in the switch without increasing the access speed of the buffer memories. The motivation is a desire to increase the number of ports on Yamada's system without increasing the access speed of the buffer memories.

6. Regarding **claim 2**, Yamada discloses a buffer control apparatus, wherein the deferred queue device queues packets/frames, which cannot be transmitted to destination ports, when the destination ports are unavailable. **(Column 4, Lines 50-55 and S16 in Figure 4A)**

7. **Claims 3-6, 8, and 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Yamanaka as applied to claim 1 above, and further in view of Merchant et al (US 6, 904, 043), hereinafter referred to as Merchant.

8. Regarding **claim 3**, the combination of Yamada and Yamanaka teaches a buffer control apparatus, wherein the deferred queue device has a means for periodically determining current status of all destination ports in the buffered switch **(Yamada Column 4, Lines 30-38 and Figure 3, element 501 Buffer Occupancy State Signal Line)**.

The combination of Yamada and Yamanaka fails to teach a deferred header queue device for storing frame information for packets/frames being deferred; and header select logic unit for determining state of the deferred queue device and supplying a valid buffer address for a deferred packet/frame which can now be sent to an available destination port.

Merchant teaches a network switch configured for switching data packets across multiple ports and uses an internal memory to store frame headers for processing by decision-making logic.

Merchant discloses a deferred header queue device for storing frame information for packets/frames being deferred **(See Figures 4 and 5)**; and header select logic unit for determining state of the deferred queue device and supplying a valid buffer address for a deferred packet/frame which can now be sent to an available destination port. **(See Column 9, Lines 50-60 and Column 10, Lines 15-29)**

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify the combination of Yamada's and Yamanaka's system by incorporating deferred header queue with a header select logic to increase processor speed in the switch without sending the actual data from storage to the switch for re-processing. The motivation is a desire to increase switch processor speed in Yamada's system and consequently increasing the number of ports it can handle.

9. Regarding **claim 4**, Yamada teaches a buffer control apparatus, wherein the deferred queue device is in one of an Initial State, a Deferred State, and a Backup State. **(Yamada teaches that there can be several level of queues or spare cell**

buffers to handle the data that can be delivered to the busy output ports as indicated in Figure 4 A in steps 12 and steps 13 and step 24 in Figure 4B)

10. Regarding **claim 5**, Yamada teaches a buffer control apparatus, wherein the buffer control device further comprises: a backup header queue device for storing frame information for packets/frames waiting to be sent to at least one destination port because the packets/frames arrived at an input port while deferred packets/frames were being sent to the at least one destination port. **(Yamada teaches that there can be several level of queues or spare cell buffers to handle the data that can be delivered to the busy output ports as indicated in Figure 4 A in steps 12 and steps 13 and step 24 in Figure 4B)**

11. Regarding **claim 6**, Yamada teaches a buffer control apparatus, wherein the buffer control device further comprises: a backup header queue device that operates in parallel with the deferred header queue for storing frame information for packets/frames waiting to be sent to at least destination port. **(Yamada teaches that there can be several level of queues or spare cell buffers to handle the data that can be delivered to the busy output ports as indicated in Figure 4 A in steps 12 and steps 13 and step 24 in Figure 4B. The spare cell buffers can be accessed in parallel.)**

12. Regarding **claim 8**, the combination of Yamada and Yamanaka teaches all aspects of the claimed invention as set forth in the rejection of claim 3 but fails to disclose a buffer control apparatus, wherein the stored frame information comprises frame header information and a starting address in the buffer memory for the packet/frame.

Merchant discloses a buffer control apparatus, wherein the stored frame information comprises frame header information and a starting address in the buffer memory for the packet/frame. **(See Column 9, Lines 50-60 and Column 10, Lines 15-29; See also Figures 4 and 5)**

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify the combination of Yamada's and Yamanaka's system by incorporating deferred header queue with a header select logic, where stored information comprises frame header information and a starting address in the buffer memory for the packet/frame, to increase processor speed in the switch without sending the actual data from storage to the switch for re-processing. The motivation is a desire to increase switch processor speed in Yamada's system and consequently increasing the number of ports it can handle.

13. Regarding **claim 9**, the combination of Yamada and Yamanaka teaches all aspects of the claimed invention as set forth in the rejection of claim 3 but fails to disclose a buffer control apparatus, wherein the stored frame information comprises frame header information and a starting address in the buffer memory for the packet/frame.

Merchant discloses a buffer control apparatus, wherein the stored frame information comprises frame header information and a starting address in the buffer memory for the packet/frame. **(See Column 9, Lines 50-60 and Column 10, Lines 15-29; See also Figures 4 and 5)**

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify the combination of Yamada's and Yamanaka's system by incorporating deferred header queue with a header select logic, where stored information comprises frame header information and a starting address in the buffer memory for the packet/frame, to increase processor speed in the switch without sending the actual data from storage to the switch for re-processing. The motivation is a desire to increase switch processor speed in Yamada's system and consequently increasing the number of ports it can handle.

14. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Yamanaka and Merchant as applied to claim 3 above, and further in view of Caldara et al (US 5, 978, 359).

The combination of Yamada, Yamanaka and Merchant teaches all aspects of the invention as set forth in the rejection of claim 3 but fails to disclose a buffer control apparatus, wherein XOFF masks are used to determine current status of all destination ports in the buffered switch.

Caldara teaches a system for eliminating cell loss in an ATM switch through the use of flow control of allocated and dynamic bandwidth and buffer.

Caldara teaches disclose a buffer control apparatus, wherein XOFF masks are used to determine current status of all destination ports in the buffered switch. **(Column 6, Lines 40-47 and see also Table 1)**

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify the combination of Yamada's, Yamanaka's and Merchant's

system by incorporating XOFF mask. The motivation is a desire to increase switch processor speed in Yamada's system by using XOFF mask it will help to reduce switch traffic by cutting back on unnecessary feedback signaling within the switch.

15. **Claims 10-13 and 15-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US 5, 455, 820) in view of Merchant et al (US 6, 904, 043), hereinafter referred to as Merchant.

16. Regarding **claim 10**, Yamada teaches a deferred queue device for temporarily deferring transmission of packets/frames to a destination port in a buffered switch and means for periodically determining current status of all destination ports in the buffered switch. **(Yamada in Figure 3 shows the deferred queue as cell buffers 140_2 and 140_3. See also Column 4, Lines 50-67.)**

Yamada fails to teach a header queue device for storing frame information for packets/frames being deferred; and header select logic unit for determining state of the deferred queue device and supplying a valid buffer address for a deferred packet/frame, which can now be sent to an available destination port.

Merchant discloses a header queue device for storing frame information for packets/frames being deferred; and header select logic unit for determining state of the deferred queue device and supplying a valid buffer address for a deferred packet/frame, which can now be sent to an available destination port. . **(See Column 9, Lines 50-60 and Column 10, Lines 15-29; See also Figures 4 and 5)**

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify the combination of Yamada's and Yamanaka's system by

incorporating deferred header queue with a header select logic unit for determining state of the deferred queue device and supplying a valid buffer address for a deferred packet/frame, to increase processor speed in the switch without sending the actual data from storage to the switch for re-processing. The motivation is a desire to increase switch processor speed in Yamada's system and consequently increasing the number of ports it can handle.

17. Regarding **claim 11**, Yamada discloses a deferred queue device, wherein the deferred queue device can be in one of an Initial State, a Deferred State, and a Backup State. **(Yamada teaches that there can be several level of queues or spare cell buffers to handle the data that can be delivered to the busy output ports as indicated in Figure 4 A in steps 12 and steps 13 and step 24 in Figure 4B)**

18. Regarding **claim 12**, Yamada disclose a deferred queue device, further comprising: a backup header queue device for storing frame information for packets/frames waiting to be sent to at least one destination port because the packets/frames arrived at an input port while deferred packets/frames were being sent to the at least one destination port. **(Yamada teaches that there can be several level of queues or spare cell buffers to handle the data that can be delivered to the busy output ports as indicated in Figure 4 A in steps 12 and steps 13 and step 24 in Figure 4B. The spare cell buffers can be accessed in parallel.)**

19. Regarding **claim 13**, Yamada discloses a deferred queue device, further comprising: a backup header queue device that operates in parallel with the deferred header queue for storing frame information for packets/frames waiting to be sent to at

least destination port. **(Yamada teaches that there can be several level of queues or spare cell buffers to handle the data that can be delivered to the busy output ports as indicated in Figure 4 A in steps 12 and steps 13 and step 24 in Figure 4B. The spare cell buffers can be accessed in parallel.)**

20. **Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Merchant as applied to claim 10 above, and further in view of Caldara et al (US 5, 978, 359), hereinafter referred to as Caldara.

The combination of Yamada and Merchant teaches all aspects of the invention as set forth in the rejection of claim 10 but fails to disclose a buffer control apparatus, wherein XOFF masks are used to determine current status of all destination ports in the buffered switch.

Caldara teaches a deferred queue device, wherein XOFF masks are used to determine current status of all destination ports in the buffered switch. **(Column 6, Lines 40-47 and see also Table 1)**

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify the combination of Yamada's and Merchant's system by incorporating XOFF mask. The motivation is a desire to increase switch processor speed in Yamada's system by using XOFF mask it will help to reduce switch traffic by cutting back on unnecessary feedback signaling within the switch.

21. Regarding **claim 15**, Yamada teaches a deferred queue device, wherein the deferred queue device queues packet/frames, which cannot be transmitted to the destination ports. **(Column 4, Lines 50-55 and S16 in Figure 4A)**

22. Regarding **claim 16**, Yamada teaches all aspects of the claimed invention as set forth in the rejection of claim 10 but fails to disclose a buffer control apparatus, wherein the stored frame information comprises frame header information and a starting address in the buffer memory for the packet/frame.

Merchant discloses a buffer control apparatus, wherein the stored frame information comprises frame header information and a starting address in the buffer memory for the packet/frame. **(See Column 9, Lines 50-60 and Column 10, Lines 15-29; See also Figures 4 and 5)**

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify the combination of Yamada's and Yamanaka's system by incorporating deferred header queue with a header select logic, where stored information comprises frame header information and a starting address in the buffer memory for the packet/frame, to increase processor speed in the switch without sending the actual data from storage to the switch for re-processing. The motivation is a desire to increase switch processor speed in Yamada's system and consequently increasing the number of ports it can handle.

23. Regarding **claim 17**, Yamada teaches all aspects of the claimed invention as set forth in the rejection of claim 12 but fails to disclose a buffer control apparatus, wherein the stored frame information comprises frame header information and a starting address in the buffer memory for the packet/frame.

Merchant discloses a buffer control apparatus, wherein the stored frame information comprises frame header information and a starting address in the buffer

memory for the packet/frame. **(See Column 9, Lines 50-60 and Column 10, Lines 15-29; See also Figures 4 and 5)**

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify the combination of Yamada's and Yamanaka's system by incorporating deferred header queue with a header select logic, where stored information comprises frame header information and a starting address in the buffer memory for the packet/frame, to increase processor speed in the switch without sending the actual data from storage to the switch for re-processing. The motivation is a desire to increase switch processor speed in Yamada's system and consequently increasing the number of ports it can handle.

24. **Claims 19-24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US 5, 455, 820) in view of Merchant et al (US 6, 904, 043), hereinafter referred to as Merchant.24.

25. Regarding **claims 19 and 23**, Yamada teaches a method, further comprising the steps of: periodically checking to determine if destination ports for deferred packets/frames are available **(Figure 4b, Step 21)**; transmitting the at least one packet/frame to destination ports when it is determined that the destination ports are available **(Figure 4b, Step 24);** and removing frame/packet identifier and memory address for the at least one transmitted packet/frame from the deferred queue **(Figure 4b, Step 26)**.

Yamada fails to teach storing a frame/packet identifier and memory address for each deferred packet/frame in a deferred header queue.

Merchant discloses storing a frame/packet identifier and memory address for each deferred packet/frame in a deferred header queue. **(See Column 9, Lines 50-60 and Column 10, Lines 15-29; See also Figures 4 and 5)**

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify Yamada's system by incorporating deferred header queue with a header select logic, where stored information comprises frame header information and a starting address in the buffer memory for the packet/frame, to increase processor speed in the switch without sending the actual data from storage to the switch for re-processing. The motivation is a desire to increase switch processor speed in Yamada's system and consequently increasing the number of ports it can handle.

26. Regarding **claim 20**, Yamada teaches all aspects of the claimed invention as set forth in the rejection of claim 18 but fails to teach a method wherein each frame/packet identifier and memory address is stored in the same order it was received.

Merchant teaches a method wherein each frame/packet identifier and memory address is stored in the same order it was received. **(See Column 9, Lines 50-60 and Figure 5)**

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify Yamada's system by incorporating deferred header queue with a header select logic, where each frame/packet identifier and memory address is stored in the same order it was received, to increase processor speed in the switch without sending the actual data from storage to the switch for re-processing. The

motivation is a desire to increase switch processor speed in Yamada's system and consequently increasing the number of ports it can handle.

27. Regarding **claim 21**, Yamada discloses a method wherein each frame/packet is transmitted to the destination port based on the oldest packet identifier at the deferred header queue for the destination port. **(This is inherent to Yamada's system as it is using a FIFO buffer. Column 4, Line 29)**

28. Regarding **claim 22**, Yamada discloses a method, further comprising the step of: transmitting at least one packet/frame to the destination port if it is determined that the destination port is available. **(Column 5, Lines 5-15)**

29. Regarding **claim 24**, Yamada discloses a method wherein each frame/packet identifier is transmitted to the destination port based on first packet received at the backup header queue for the destination port. **(Yamada teaches that the deferred packet is transmitted from the spare cell buffers that serve as deferred queue to the destination port when the overflow clears. See Column 5, Lines 1-5)**

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Habte Mered whose telephone number is 571 272 6046. The examiner can normally be reached on Monday to Friday 9:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571 272 3088. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HM
08-05-2005

JOHN PEZZLO
PRIMARY EXAMINER